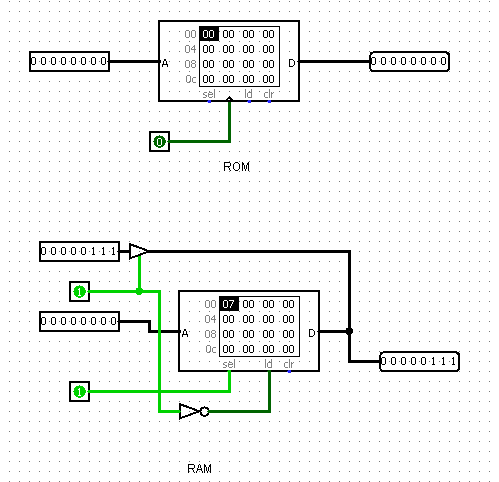
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CS226- Lab 13

Q1: Simulate the following RAM and ROM modules using logic-sim. Simulate for various ROM/RAM sizes.

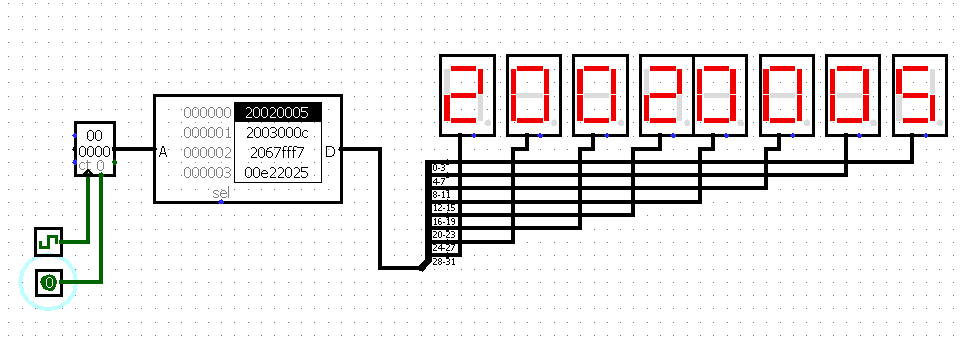
**(10 points)**

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Q2: Design and simulate a 2M × 32 memory system using 512K × 8 memory chips?

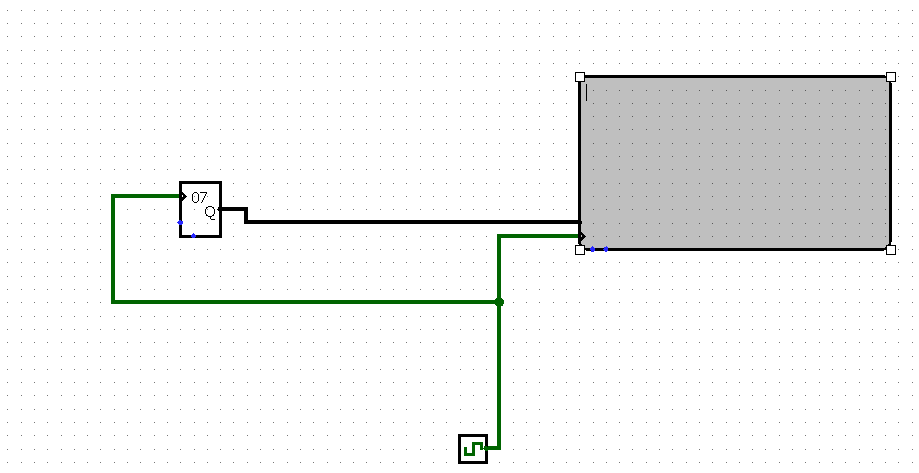
**(15 points)**

**Q4: Design a 16Mx32 bit memory blocks. Load the memory with given data (memory.dat) and test using appropriate test environment. ( one sample test set up given)**



**Q4: Design a 230byte ( 1Gx 8 bit) memory system using 16Mx1 bit memory blocks and simulate with various test data.**

**Q5: Design a 1Mx7 bit memory and write random data and read out data in every clock cycle and display using TTY (sample display design is shown)**



Submit your .circ file containing your implementations. Show the simulations to TAs.

Email: The simulation files p1.circ, p2.circ, p3.circ and p4.circ , to : [cs225.iitp@gmail.com](mailto:cs225.iitp@gmail.com)

(use email subject Lab13\_Logicsim\_your roll number).

This work is due on: : 15th April 2019